

PTO-1449 REPRODUCED  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  March 2, 2004  (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.1006-012	CONT. OF APPLICATION NO. 10/ <del>463,194</del> 791-437	
	APPLICANT Valerie L. Lines		
	FILING DATE	CONFIRMATION NO.	GROUP 2824

U.S. PATENT DOCUMENTS				
EXAM- INER INI- TIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
PL	AA	4,189,782	02/19/1980	Dingwall
	AB	4,442,481	04/10/1984	Brahmbhatt
	AC	4,583,157	04/15/1986	Kirsch et al.
	AD	4,689,504	08/25/1987	Raghunathan et al.
	AE	4,692,638	09/08/1987	Stiegler
	AF	4,716,313	12/29/1987	Hori et al.
	AG	4,730,132	03/08/1988	Watanabe et al.
	AH	4,814,647	03/21/1989	Tran
	AI	4,857,763	08/15/1989	Sakurai et al.
	AJ	4,878,201	10/31/1989	Nakaizumi
	AK	4,888,738	12/19/1989	Wong et al.
	AA2	5,010,259	04/23/1991	Inoue et al.
	AB2	5,031,149	07/09/1991	Matsumoto et al.
	AC2	5,038,327	08/06/1991	Akaogi
	AD2	5,150,325	09/22/1992	Yanagisawa et al.
	AE2	5,347,488	09/13/1994	Matsubita
	AF2	5,351,217	09/27/1994	Jeon
	AG2	5,377,156	12/27/1994	Watanabe et al.
	AH2	4,814,647	03/21/1989	Tran
	AI2	5,031,149	07/09/1991	Matsumoto et al.
	AJ2	5,038,327	08/06/1991	Akaogi
	AK2	5,751,643	05/12/1998	Lines
	AA3	4,344,005	08/10/1982	Stewart
	AB3	5,023,465	06/11/1991	Douglas et al.
✓	AC3	3,801,831	04/02/1974	Dame
PL	AD3	3,942,047	03/02/1976	Buchanan

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PL	AE3	3,980,899	09/14/1976	Shimada et al.
	AF3	4,000,412	12/28/1976	Rosenthal et al.
	AG3	4,039,862	08/02/1977	Dingwall et al.
	AH3	4,080,539	03/21/1978	Stewart
	AI3	4,208,595	06/17/1980	Gladstein
	AJ3	4,271,461	06/02/1981	Hoffmann et al.
	AK3	4,279,010	07/14/1981	Morihisa
	AA4	4,307,333	12/22/1981	Hargrove
	AB4	4,403,158	09/06/1983	Slemmer
	AC4	4,433,253	02/21/1984	Zapisek
	AD4	4,486,670	12/04/1984	Chan et al.
	AE4	4,543,500	09/24/1985	McAlexander, et al.
	AF4	4,581,546	04/08/1986	Allan
	AG4	4,621,315	11/04/1986	Vaughn et al.
	AH4	4,628,214	12/09/1986	Leuschner
	AI4	4,642,798	02/10/1987	Rao
	AJ4	4,656,373	04/07/1987	Plus
	AK4	4,670,861	06/02/1987	Shu et al.
	AA5	4,697,252	09/29/1987	Furuyama et al.
	AB5	4,730,132	03/08/1988	Watanabe et al.
	AC5	4,740,918	04/26/1988	Okajima et al.
	AD5	4,751,679	06/14/1988	Dehganpour
	AE5	4,798,977	01/17/1989	Sakui et al.
✓	AF5	4,807,190	02/21/1989	Ishii et al.
PL	AG5	4,811,304	03/07/1989	Matsuda et al.

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PL	AH5	4,837,462	06/06/1989	Watanabe et al.
	AI5	4,843,256	06/27/1989	Scade et al.
	AJ5	4,873,673	10/10/1989	Hori et al.
	AK5	4,881,201	11/14/1989	Sato et al.
	AA6	4,906,056	03/06/1990	Taniguchi
	AB6	4,951,259	08/21/1990	Sato et al.
	AC6	4,961,007	10/02/1990	Kumanoya et al.
	AD6	5,018,107	05/21/1991	Yoshida
	AE6	5,023,465	06/11/1991	Douglas et al.
	AF6	5,038,325	08/06/1991	Douglas et al.
	AG6	5,059,815	10/22/1991	Bill et al.
	AH6	5,086,238	02/04/1992	Watanabe et al.
	AI6	5,101,381	03/31/1992	Kouzi
	AJ6	5,103,113	04/07/1992	Inui et al.
	AK6	5,159,215	10/27/1992	Murotani
	AA7	5,197,033	03/23/1993	Watanabe et al.
	AB7	5,208,776	05/04/1993	Nasu et al.
	AC7	5,262,999	11/16/1993	Etoh et al.
	AD7	5,264,743	11/23/1993	Nakagome et al.
	AE7	5,276,646	01/04/1994	Kim et al.
	AF7	5,297,097	03/22/1994	Etoh et al.
	AG7	5,307,315	04/26/1994	Oowaki et al.
	AH7	5,311,476	05/10/1994	Kajimoto et al.
	AI7	5,323,354	06/21/1994	Matsumoto et al.
✓	AJ7	5,912,564	06/15/1999	Kai et al.
PL	AK7	4,612,462	09/16/1986	Asano et al.

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PL	AA8	5,196,996	03/23/1993	Oh
	AB8	4,001,606	01/04/1977	Dingwall
	AC8	4,037,114	07/19/1977	Stewart et al.
	AD8	4,533,843	08/06/1985	McAlexander, III et al.
	AE8	4,616,303	10/07/1986	Mauthe
	AF8	4,639,622	01/27/1987	Goodwin et al.
	AG8	4,820,941	04/11/1989	Dolby et al.
	AH8	4,823,318	04/18/1989	D'Arrigo et al.
	AJ8	5,151,616	09/29/1992	Komuro
	AJ8	3,761,899	09/25/1973	McKenny et al.
	AK8	4,216,390	08/05/1980	Stewart
	AA9	4,471,290	09/11/1984	Yamaguchi
	AB9	4,733,108	03/22/1988	Truong
	AC9	5,245,576	09/14/1993	Foss et al.
	AD9	4,678,941	07/07/1987	Chao et al.
	AE9	4,344,003	08/10/1982	Harmon et al.
	AF9	5,602,771	02/11/1997	Kajigaya et al.
	AG9	5,828,620	10/27/1998	Foss et al.
	AH9	6,236,581	05/22/2001	Foss et al.
	AJ9	4,061,929	12/06/1977	Asano
	AJ9	4,029,973	06/14/1977	Kobayashi et al.
	AK9	4,045,691	08/30/1977	Asano
	AA10	4,330,852	05/18/1982	Redwine et al.
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
PL	AR	Kitsukawa, Goro, <i>et al.</i> , "An Experimental 1-Mbit BiCMOS DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-22, No. 5, October 1987, pp. 657-662.
	AS	Ishihara, <i>et al.</i> , "256k CMOS Dynamic RAM With Static Column Mode of Cycle Time of 50 ns," <i>Nikkei Electronics</i> , February 11, 1985, pp 243-263.
	AT	Kitsukawa, Goro, <i>et al.</i> , "A 1-Mbit BiCMOS DRAM Using Temperature-Compensation Circuit Techniques," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 3, June 1989, pp. 597-601.
	AU	Kitsukawa, Goro, <i>et al.</i> , "A 23-ns 1-Mb BiCMOS DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No 5, October 1990, pp. 1102-1111.
	AV	Nakagome, Yoshinobu, <i>et al.</i> , "An Experimental 1.5-V 64-Mb DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 4, April 1991, pp. 465-472.
	AW	Fujii, Syuso, <i>et al.</i> , "A 45-ns 16-Mbit DRAM with Triple-Well Structure," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 5, October 1989, pp. 1170-1174.
	AX	Gillingham, Peter, <i>et al.</i> , "High-Speed, High-Reliability Circuit Design for Megabit DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 8, August 1991, pp. 1171-1175.
	AY	Fujii, S., <i>et al.</i> , "A 45ns 16Mb DRAM with Triple-Well Structure," <i>1989 IEEE International Solid-State Circuits Conference (ISSCC 89)</i> , Session 16: DYNAMIC RAMs, FAM 16.6, pp. 248-249, February 1989.
	AZ	Lu, N.C.C., <i>et al.</i> , "A 20-ns 128-kbit x 4 High-Speed DRAM with 330-Mbit/s Data Rate", <i>IEEE Journal of Solid-State Circuits</i> , V. 23, No.5, pp. 1140-1149, October 1988.
	AR2	Lu, N.C.C., <i>et al.</i> , "A 20ns 512Kb DRAM with 83MHz Page Operation" <i>1989 IEEE International Solid-State Circuits Conference (ISSCC 88)</i> , Session XVI: DYNAMIC MEMORY, FAM 16.3, February 1988.
	AS2	IBM Technical Disclosure Bulletin, "High Performance Complementary Decoder/Driver Circuit," V. 29, No. 6, November 1986, pp. 2390-2394.
	AT2	IBM Technical Disclosure Bulletin, "Improved Decoder Circuits for CMOS Memory Arrays," V. 30, No. 2, July 1987, pp. 664-666.
✓ PL	AU2	"An Analysis of Toshiba TC511000/TC511001 CMOS 1Mx1 DRAMs," (Author Unknown), MOSAID Inc. pp. 29-36, 145-159, August 1986.

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PL	AV2	Bursky, D., "Memory ICs," <i>Electronic Design</i> , V. 36, No. 4, pp. 71-81, February 1988.
	AW2	Kitsukawa, G., <i>et al.</i> , "A 1-M BiCMOS DRAM Using Temperature- Compensation Circuit Technique," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 3, pp. 597-601, June 1989.
	AX2	Watanabe, T., <i>et al.</i> , "Comparison of CMOS and BiCMOS 1-Mbit DRAM Performance," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 3, pp. 771-778, June 1989.
	AY2	Nakagome, Y., <i>et al.</i> , "An Experimental 1.5-V 64-Mb DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 4, pp. 465-472, April 1991.
	AZ2	Nakagome, Y., <i>et al.</i> , "A 1.5V Circuit Technology for 64Mb DRAMs," <i>1990 Symposium on VLSI Circuits</i> , Honolulu, Hawaii, pp. 17-18, June 1990.
	AR3	Bursky, D., "Digital Technology," <i>Electronic Design</i> , V. 40, No. 4, pp. 48-61, February 1992.
	AS3	Schematics of Micron 1Mx4 DRAM MT4C4001DJ-8
	AT3	Aoki, Masakazu, <i>et al.</i> , "A 1.5V DRAM for Battery-Based Applications," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 5, October 1989, pp. 1206-1212.
	AU3	Aoki, Masakazu, <i>et al.</i> , "New DRAM Noise Generation Under Half- $V_{CC}$ Precharge and its Reduction Using a Transposed Amplifier," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 4, August 1989, pp. 889-894.
	AV3	Arimoto, Kazutami, <i>et al.</i> , "A 60-ns 3.3-V-Only 16-Mbit DRAM with Multipurpose Register," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 5, October 1989, pp. 1184-1189.
	AW3	Arimoto, Kazutami, <i>et al.</i> , "A Speed-Enhanced DRAM Array Architecture with Embedded ECC," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 1, February 1990, pp. 11-17.
	AX3	Asakura, Mikio, <i>et al.</i> , "An Experimental 1-Mbit Cache DRAM with ECC," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 1, February 1990, pp. 5-10.
PL	AY3	Eldin, A.G., <i>et al.</i> , "New Dynamic Logic and Memory Circuit Structures for BiCMOS Technologies," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-22, No. 3, June 1987, pp. 450-453.

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PL	AZ3	Fujii, Syuso, <i>et al.</i> , "A 50- $\mu$ A Standby 1Mx1/256Kx4 CMOS DRAM with High-Speed Sense Amplifier," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-21, No. 5, October 1986, pp. 643-648.
	AR4	Furuyama, Tohru, <i>et al.</i> , "An Experimental 4-Mbit CMOS DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-21, No. 5, October 1986, pp. 605-611.
	AS4	Hori, Ryoichi, <i>et al.</i> , "An Experimental 1 Mbit DRAM Based on High S/N Design," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-19, No. 5, October 1984, pp. 634-640.
	AT4	Gray, Paul R., <i>et al.</i> , "MOS Operational Amplifier Design – A Tutorial Overview," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-17, No. 6, December 1982, pp. 969-982.
	AU4	Horiguchi, Masashi, <i>et al.</i> , "A Tunable CMOS-DRAM Voltage Limiter with Stabilized Feedback Amplifier," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 5, October 1990, pp. 1129-1135.
	AV4	Itoh, Kiyoo, "Trends in Megabit DRAM Circuit Design," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 3, June 1990, pp. 778-789.
	AW4	Kimura, Katsutaka, <i>et al.</i> , "A 65-ns 4-Mbit CMOS DRAM with a Twisted Driveline Sense Amplifier," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-22, No. 5, October 1987, pp. 651-656.
	AX4	Masuoka, Fujio, <i>et al.</i> , "A 256-kbit Flash E <sup>2</sup> PROM Using Triple-Polysilicon Technology," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-22, No. 4, August 1987, pp. 548-552.
	AY4	Miyamoto, Jun-Ichi, <i>et al.</i> , "An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-21, No. 5, October 1986, pp. 852-861.
	AZ4	Momodomi, Masaki, <i>et al.</i> , "An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 5, October 1989, pp. 1238-1243.
	AR5	Nakagome, Yoshinobu, <i>et al.</i> , "Circuit Techniques for 1.5–3.6-V Battery-Operated 64-Mb DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 7, July 1991, pp. 1003-1010.
PL	AS5	Ohta, Kiyoto, <i>et al.</i> , "A 1-Mbit DRAM with 33-MHz Serial I/O Ports," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-21, No. 5, October 1986, pp. 649-654.

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PL	AT5	Saito, Shozo, <i>et al.</i> , "A 1-Mbit CMOS DRAM with Fast Page Mode and Static Column Mode," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-20, No. 5, October 1985, pp. 903-908.
	AU5	Samachisa, Gheorghe, <i>et al.</i> , "A 128K Flash EEPROM Using Double-Polysilicon Technology," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-22, No. 5, October 1987, pp. 676-683.
	AV5	Scheuerlein, Roy E., <i>et al.</i> , "Shared Word Line DRAM Cell," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-19, No. 5, October 1984, pp. 640-645.
	AW5	Takada, Masahide, <i>et al.</i> , "A 4-Mbit DRAM with Half-Internal-Voltage Bit-Line Precharge," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-21, No. 5, October 1986, pp. 612-617.
	AX5	Takeshima, Toshio, <i>et al.</i> , "Voltage Limiters for DRAM's with Substrate-Plate-Electrode Memory Cells," <i>IEEE Journal of Solid-State Circuits</i> , V. 23, No. 1, February 1988, pp. 48-52.
	AY5	Witters, Johan S., <i>et al.</i> , "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits," <i>IEEE Journal of Solid-State Circuits</i> , V. 24, No. 5, October 1989, pp. 1372-1380.
	AZ5	Horiguchi, Masashi, <i>et al.</i> , "Dual-Operating-Voltage Scheme for a Single 5-V 16-Mbit DRAM," <i>IEEE Journal of Solid-State Circuits</i> , V. 23, No. 5, October 1988, pp. 1128-1133.
	AR6	Scheuerlein, Roy E., <i>et al.</i> , "Offset Word-Line Architecture for Scaling DRAM's to the Gigabit Level," <i>IEEE Journal of Solid-State Circuits</i> , V. 23, No. 1, February 1988, pp. 41-47.
	AS6	Gray, Paul R., <i>et al.</i> , <u>Analog MOS Integrated Circuits, II</u> , IEEE PRESS, 1988, pp. iv-vii, 22-23.
	AT6	Elmasry, Mohamed, editor. <u>Digital MOS Integrated Circuits II with Applications to Processors and Memory Design</u> , IEEE PRESS, 1992.
	AU6	Wang, Niantu, <u>Digital MOS Integrated Circuits - Design for Applications</u> , Prentice Hall, 1990, pp. 240-245.
	AV6	Texas Instruments, Memory Products Development, "16Mbit DRAM Crib Notes," July 1990, pp. 12-13.
PL	AW6	Martin, Ken, <i>et al.</i> , "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters," <i>IEEE Transactions on Circuits and Systems</i> , V. CAS-28, No. 8, August 1981, pp.134-141.

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PL	AX6	Johns, David A., <i>et al.</i> , <u>Analog Integrated Circuit Design</u> , John Wiley & Sons, Inc., 1997, pp. 408, 410-411, 442-443.
	AY6	Keeth, Brent, <i>et al.</i> , <u>DRAM Circuit Design</u> , Chapter 2, "The DRAM Array," John Wiley & Sons, Inc., 2000, pp. 35-68.
	AZ6	Reverse Engineering report – "An Analysis of the Toshiba TC511000/TC511001 CMOS 1Mx1 DRAMs," MOSAID, August 1986.
	AR7	Reverse Engineering full report – "An Analysis of the Toshiba TC511000/TC511001 CMOS 1Mx1 DRAMs," MOSAID, August 1986.
	AS7	Reverse Engineering report – Samsung KM44C4100BS-7, 6 pgs.
	AT7	Reverse Engineering report – "A Design Analysis of the TMS4164," MOSAID, August 1987.
	AU7	Reverse Engineering report – "An Analysis of the i2164A," MOSAID, April 1982.
	AV7	Reverse Engineering report – Samsung KM44S64230At-GL.
	AW7	Center, Ronald P., <i>et al.</i> "A Fault-Tolerant 64K Dynamic RAM," 1979 <i>IEEE International Solid-State Circuits Conference, (ISSCC 79)</i> , Session XII: DYNAMIC MEMORIES, pp. 150-151 and 290, (February 1979).
	AX7	Hoffman, William K., <i>et al.</i> , "An 8Kb Random-Access Memory Chip Using the One-Device FET Cell," <i>IEEE Journal of Solid-State Circuits</i> , V. SC-8, No. 5, October 1973, pp. 298-305.
PL	AY7	Komatsuzaki, K., <i>et al.</i> , "Circuit Techniques for a Wide Word I/O Path 64 Meg DRAM," 1991 <i>IEEE Symposium on VLSI Circuits</i> , Session 14: Dynamic RAM II, May 30-June 1, 1991, pages 133-134.

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